

Memory Signal Integrity Report

- ❖ Foxconn_SKT
- ❖ K18X001.00
- ❖ H5AN8G6NDJR-VKC

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- Released Date : **2023-11-02**

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System History

Release Date	Contents	Remarks
2023-11-02	H5AN8G6NDJR-VKC	U3

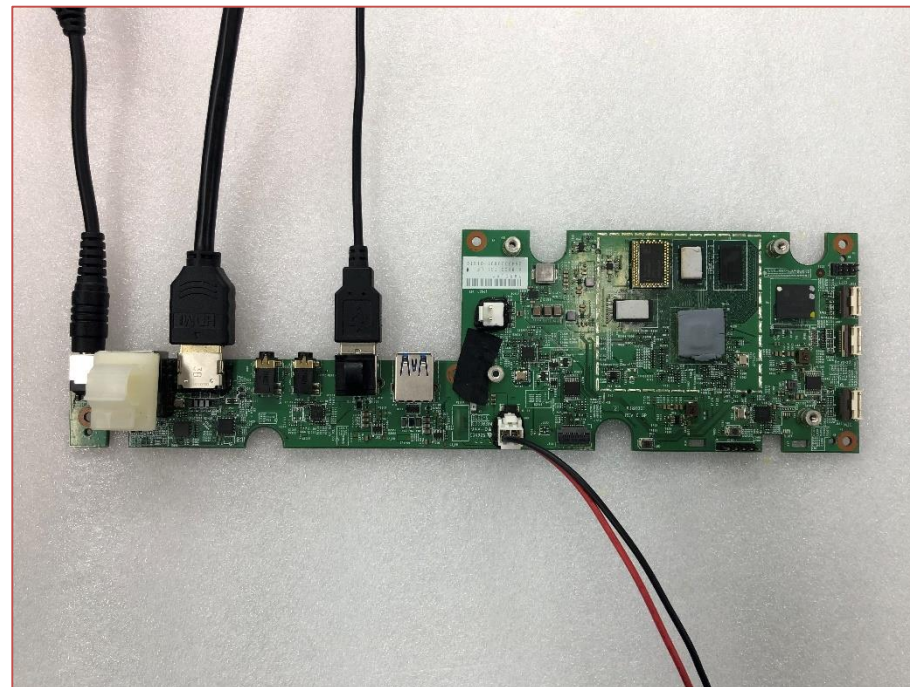
■ System & Memory Information

Model Name	K18X001.00
Application type	OTT STB+AI SOUND Bar
PCB Number and Revision	V135
Chipset	Synaptics VS-550
BIOS Version & Date	-
DRAM Part Number	H5AN8G6NDJR-VKC
DRAM Operating Frequency	1333MHz (DDR4-2666)
DRAM Density	8Gb
DRAM pieces	2ea
DRAM Width	x16

■ Equipment & Test Condition

Oscilloscope	KEYSIGHT DSAZ254A
Probes	1169B
Temperature	25°C
VDD / Vref-CA	1.200V / 0.600V

■ System picture



Summary & Conclusion

Judgment & Summary

PASS

- The clock period time of this system is 0.836ns and operating frequency is about 1196MHz.
So, we applied with DDR4-2400 criteria value of JEDEC standard.

Measurement Item	Result	Remark
Power Up Sequence Check	Spec In.	- No problem.
Power Noise Check	Spec In.	- No problem.
Signal Integrity Check	Spec In.	- No problem.

Power Up Signal Check Result

■ Power-up Initialization Sequence



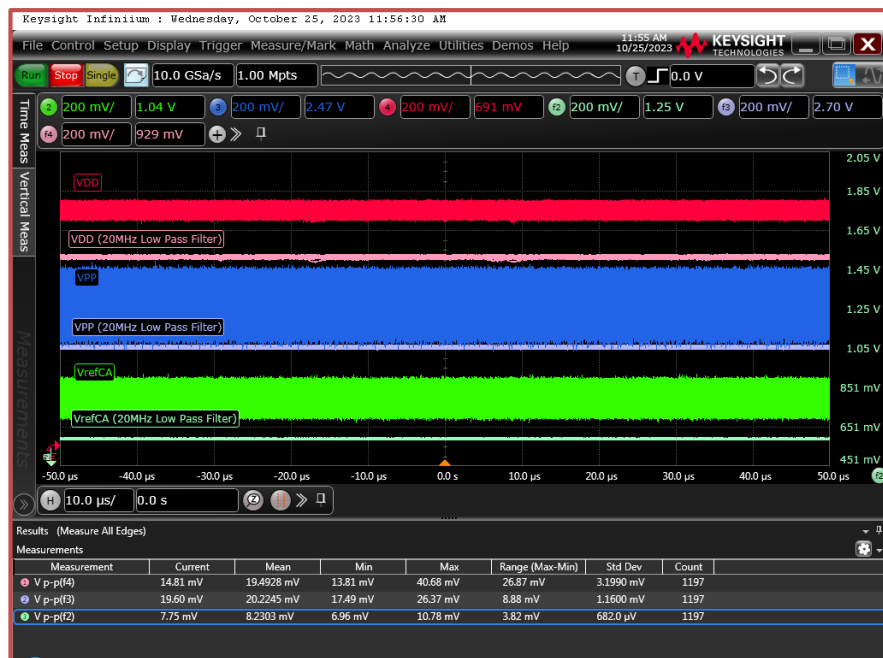
■ VDD Up Time



Parameter	Spec	Measurement	Result
RESET# needs to be maintained for minimum 200us with stable power.	Min : 200us	219.419ms	Spec. in
After RESET# is de-asserted, wait for another 500us until CKE becomes active.	Min : 500us	526.815us	Spec. in
tCKSRX	Min : 5nCK, 10ns	18.184ms	Spec. in
VDD Up Time	-	197.397ms	-

Power Noise Check Result

■ VDD / VPP / Vref_CA - with DRAM stress test

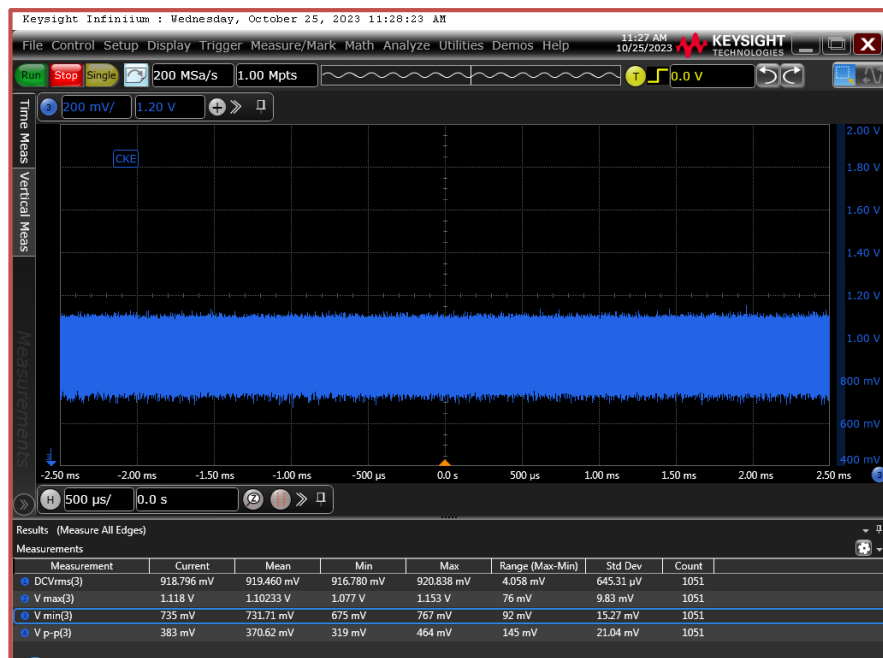


Parameter	Spec (AC+DC)	Peak to Peak	Remark
VDD	TBD	41mV	-
VPP	TBD	26mV	-
Vref-CA	≤ 24mV (VDD±1%)	11mV	Spec. in

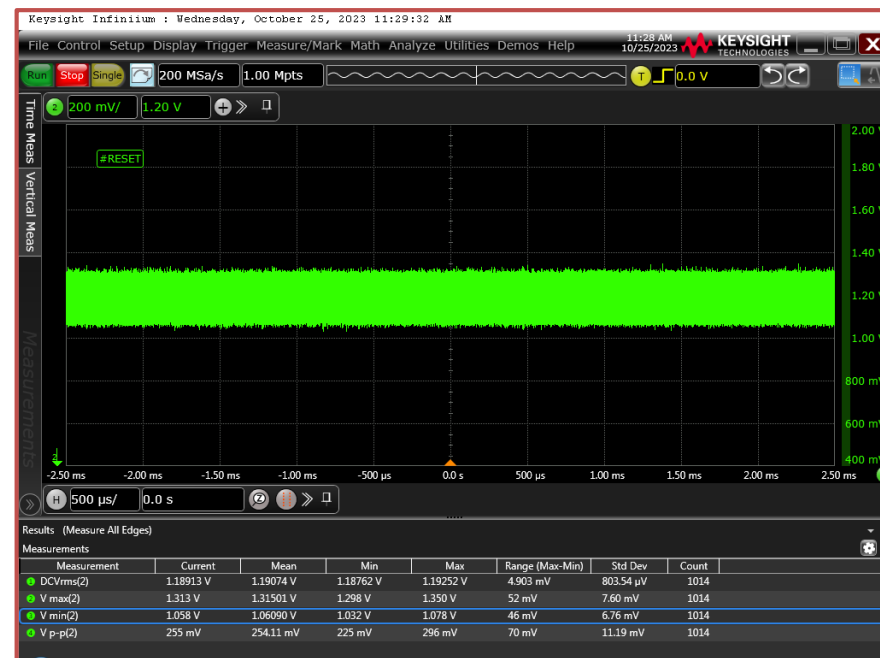
* SK hynix measured VDD/ VPP / Vref_CA including AC+DC (Low Pass Filter 20MHz) noise.

CKE & /RESET Signal Check Result

■ CKE Level in System Operation



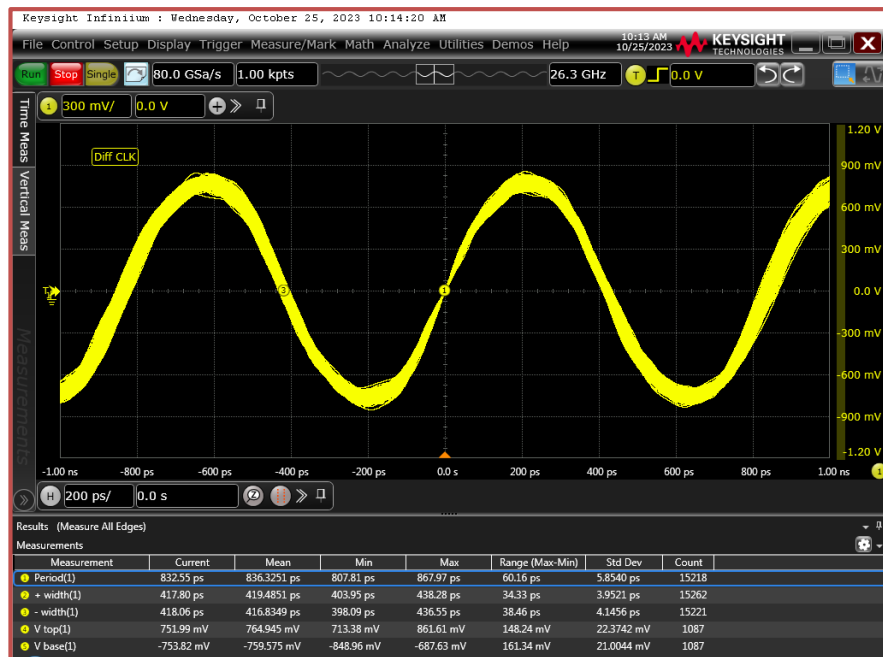
■ /RESET Level in System Operation



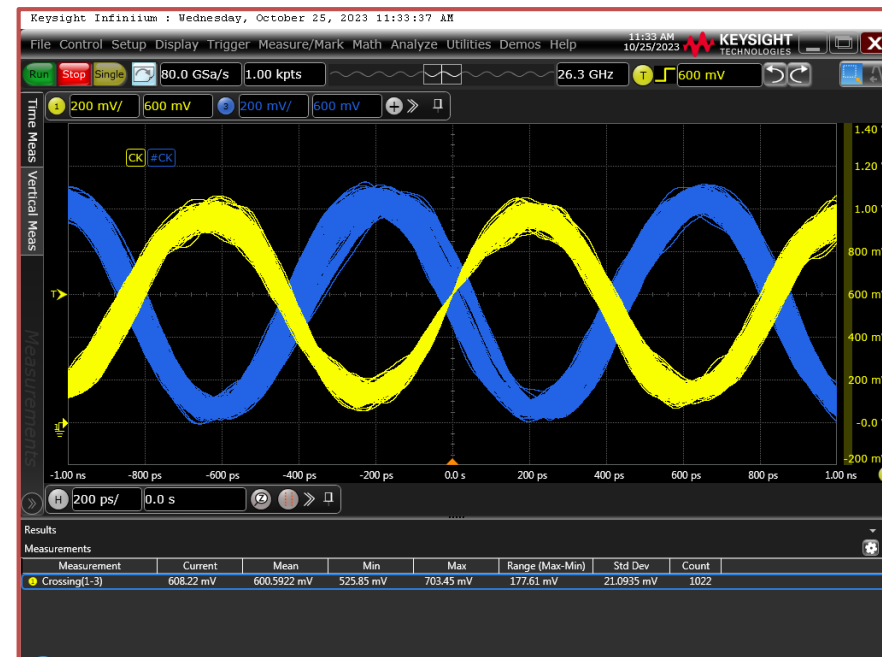
Parameter	Measurement	Remark
CKE Level	Vmin : 675mV	Power-down & Self-refresh mode not used.
/RESET Level	Vmin : 1032mV	High state stable

Signal Integrity Test Result (Clock)

■ Clock with differential



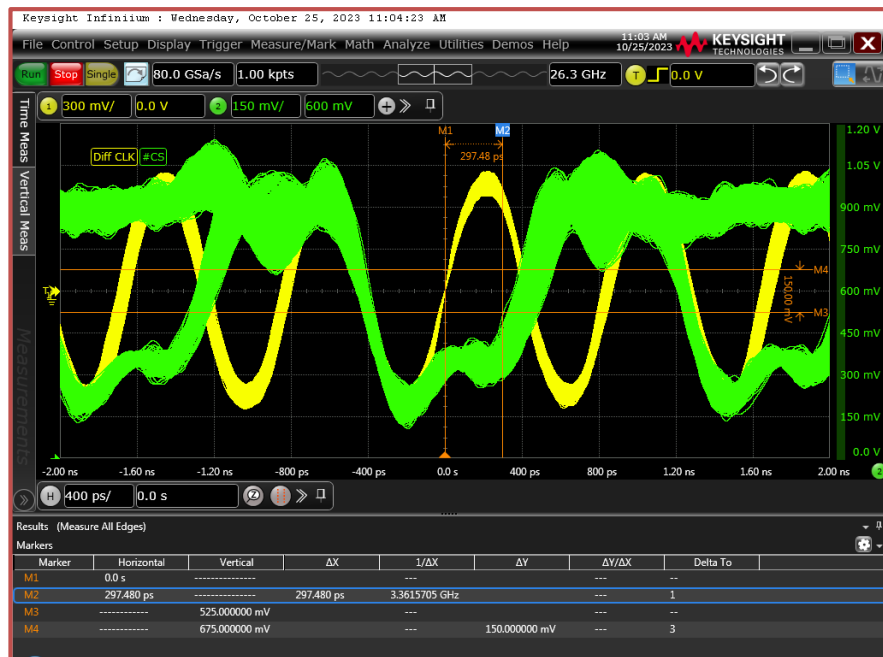
■ Clock VIX



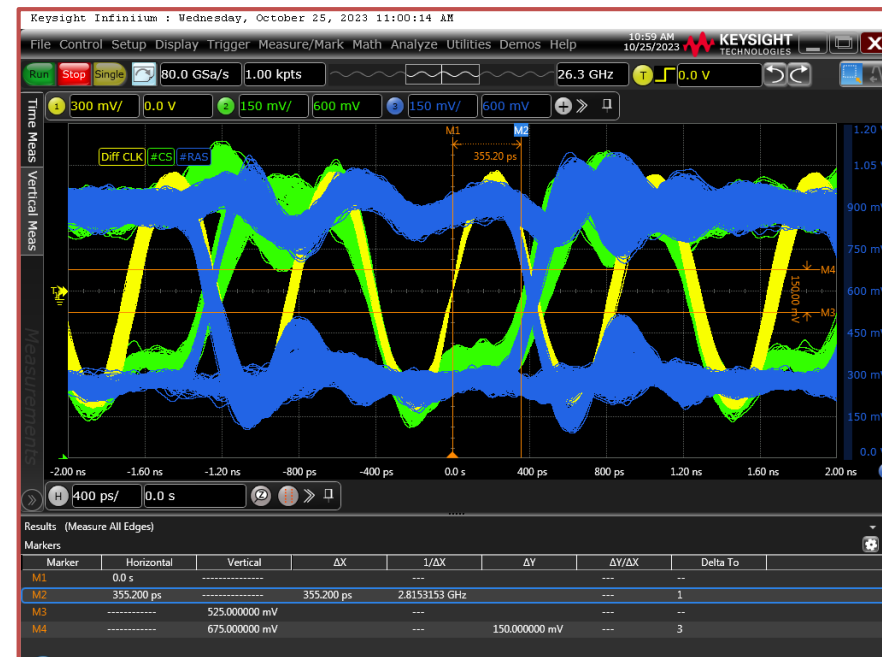
Parameter	Spec.		Measurement	Remark
	Min	Max		
Clock Cycle Time (tCK)	0.833ns	0.937ns	0.836ns	Spec. in
Clock High Level Width (tCH)	401ps(0.48tCK)	435ps(0.52tCK)	419ps (0.502tCK)	Spec. in
Clock Low Level Width (tCL)	401ps(0.48tCK)	435ps(0.52tCK)	417ps (0.498tCK)	Spec. in
Clock Period Jitter (JIT_per)	-42ps	42ps	-29 / 32	Spec. in
VIH diff(ac)	0.200V	-	0.765V	Spec. in
VIL diff(ac)	-	-0.200V	-0.760V	Spec. in
Clock VIX	0.480V	0.720V	0.526V / 0.703V	Spec. in

Signal Integrity Test Result (Command / Address)

■ CS#_U3



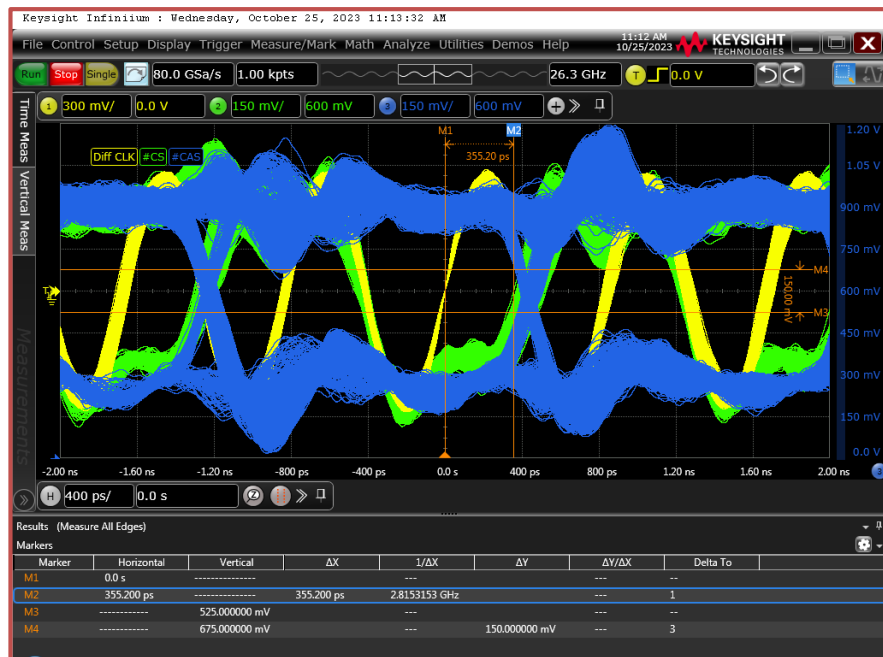
■ RAS#_U3



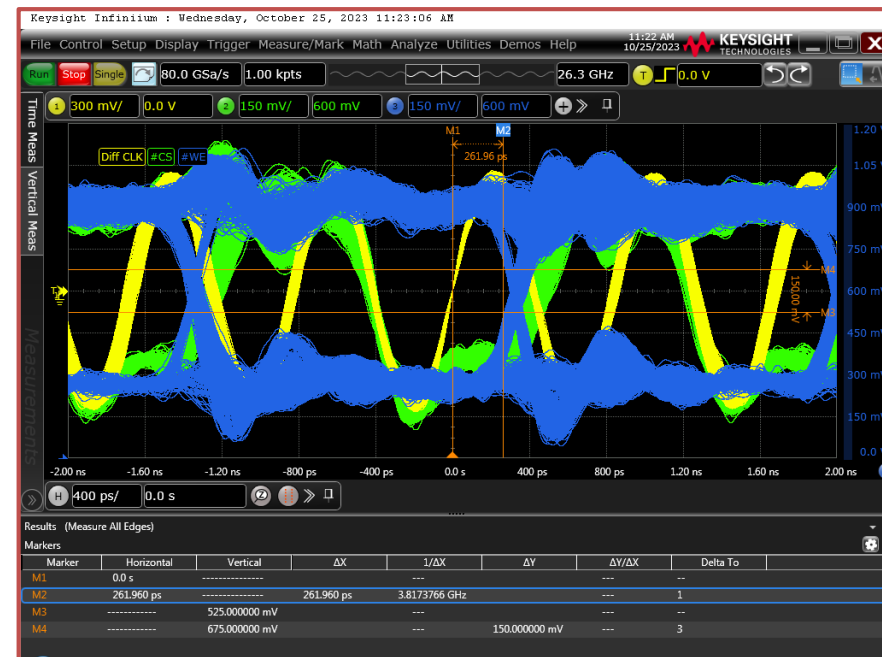
Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CS#	RAS#	
tIS(Base)	62 ps	-	351ps	746ps	Spec. in
tIH(Base)	87 ps	-	297ps	355ps	Spec. in

Signal Integrity Test Result (Command / Address)

■ CAS#_U3



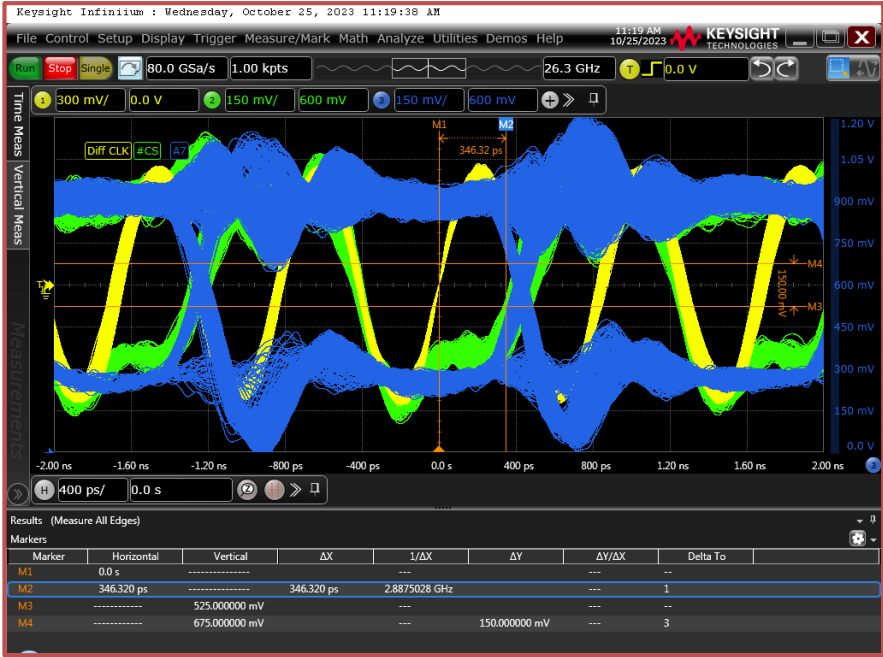
■ WE#_U3



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CAS#	WE#	
tIS(Base)	62 ps	-	755ps	1225ps	Spec. in
tIH(Base)	87 ps	-	355ps	262ps	Spec. in

Signal Integrity Test Result (Command / Address)

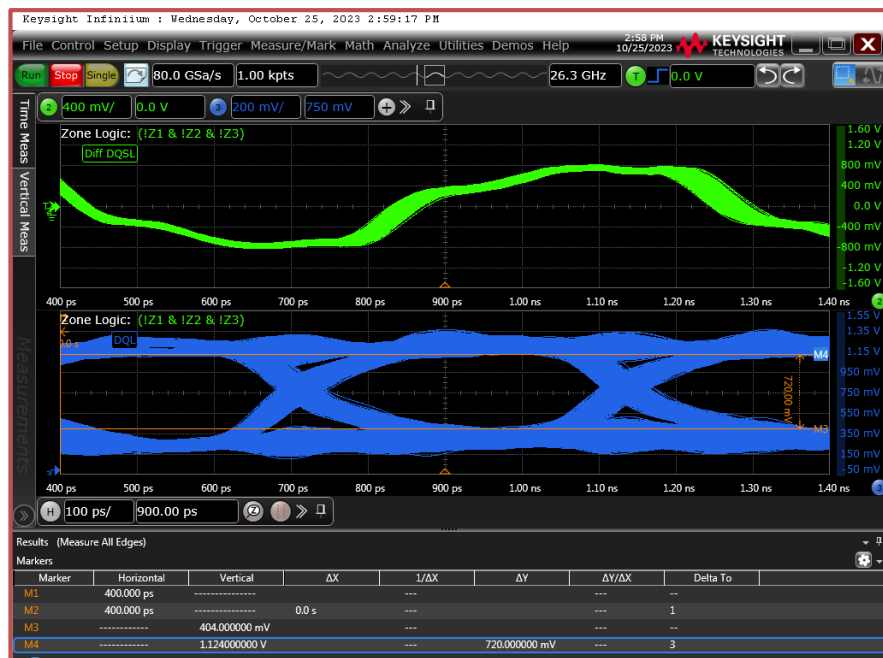
■ ADD7_U3



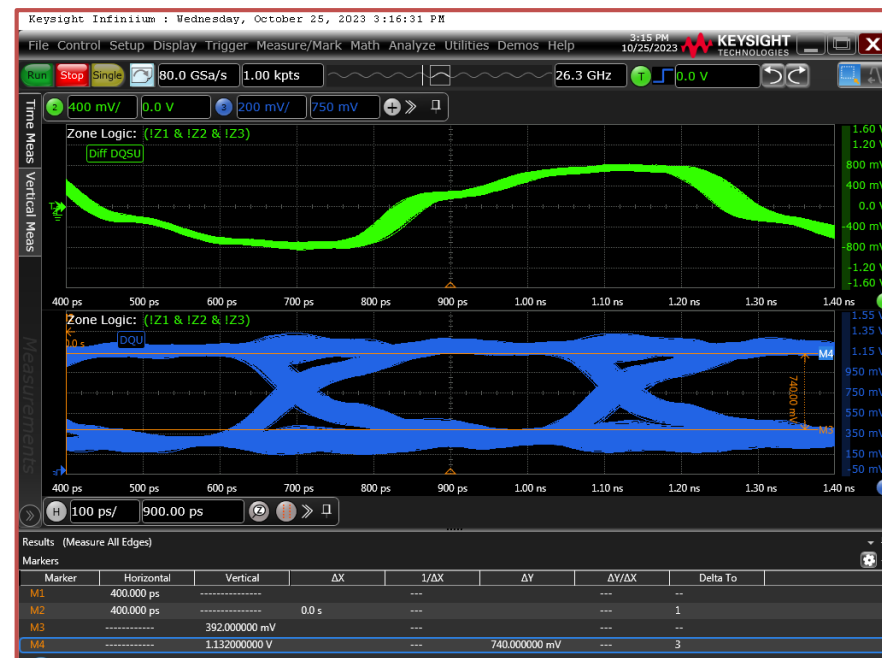
Parameter	Spec.		Measurement	Remark
Unit : ps	Min	Max	ADD7	
tIS(Base)	62 ps	-	764ps	Spec. in
tIH(Base)	87 ps	-	346ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ VIHL_AC_U3_DQL



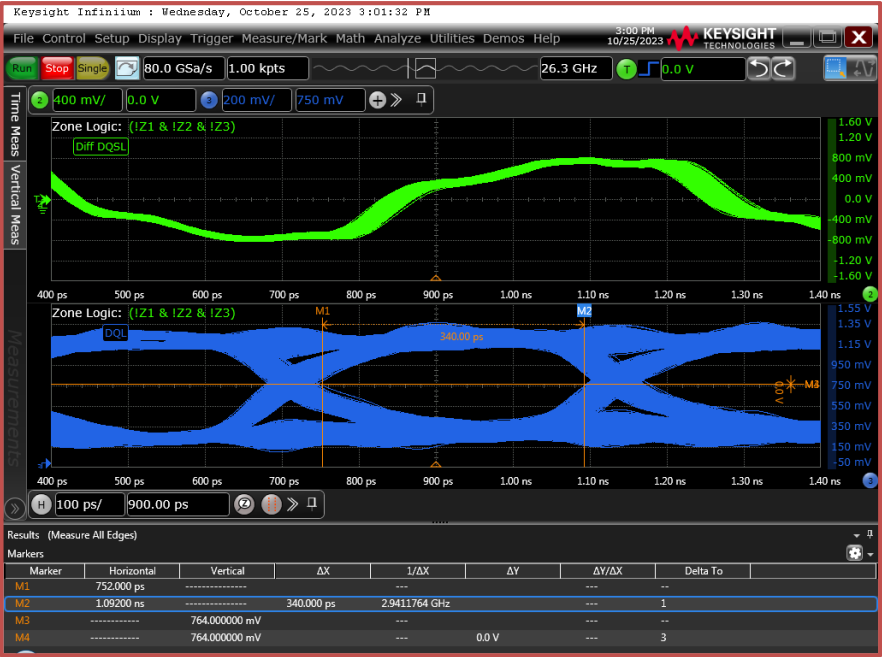
■ VIHL_AC_U3_DQU



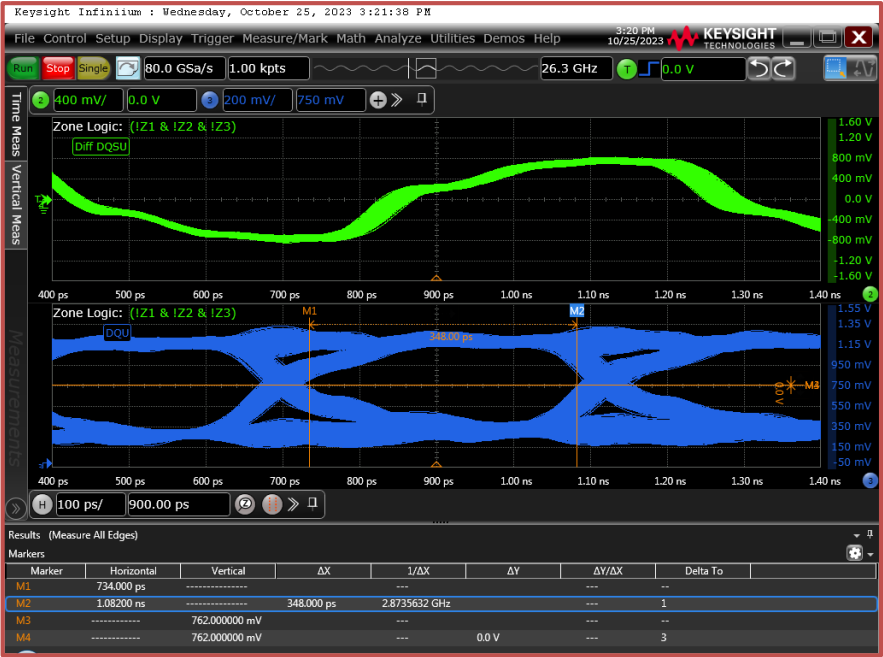
Parameter	Spec.		Measurement		Remark
Unit : mV	Min	Max	DQL	DQU	
VIHL	160 mV	-	720mV	740mV	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ TdIPW_U3_DQL



■ TdIPW_U3_DQU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQL	DQU	
TdIPW	234 ps (0.58 UI)	-	340ps	348ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

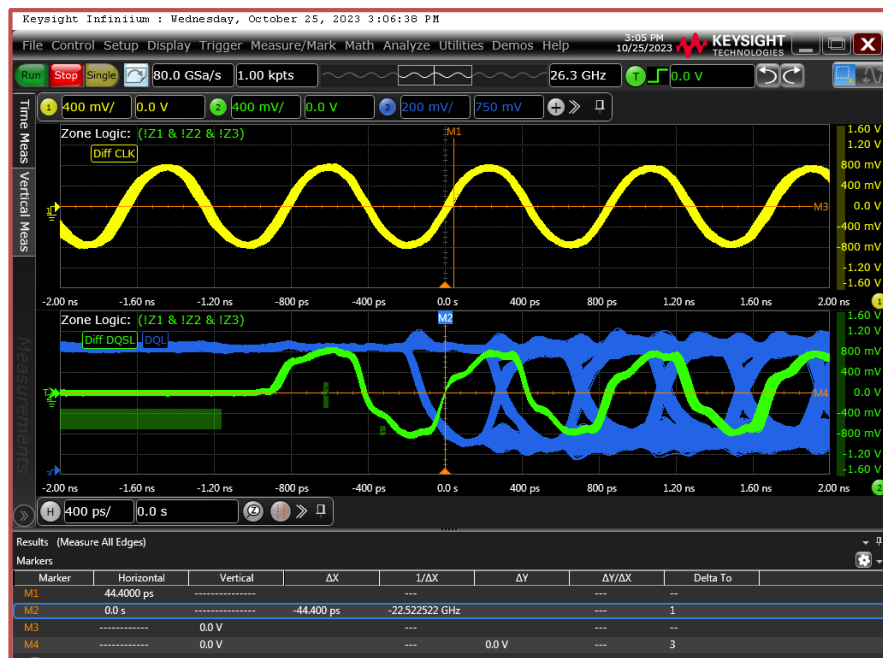
■ TdIVW_total / VdIVW_total_U3_DQL ※ : Spec. Zone ■ TdIVW_total / VdIVW_total_U3_DQU



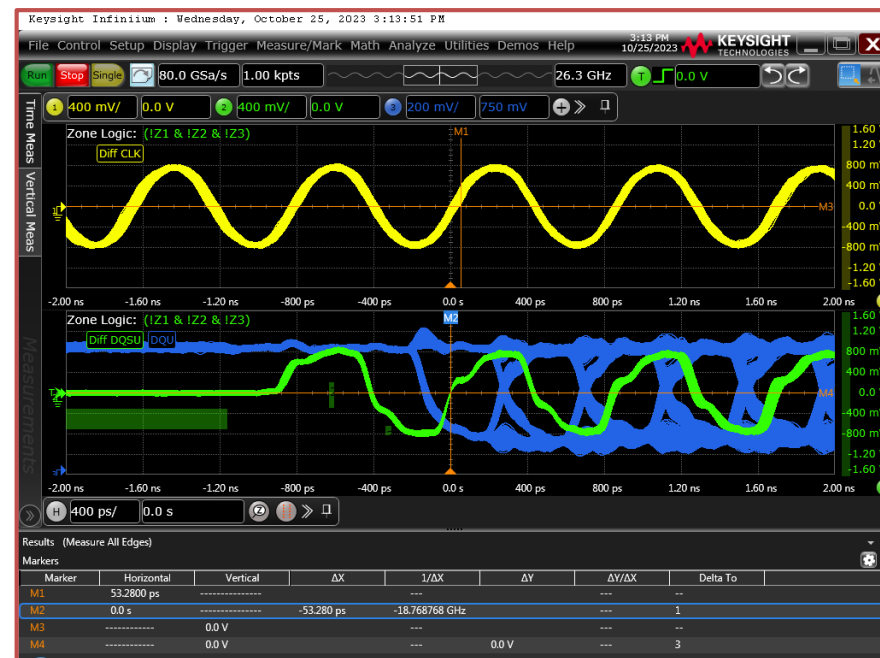
Parameter	Spec.		Measurement		Remark
Unit : ps, mV	Min	Max	DQL	DQU	
TdIVW_total	-	81 ps (0.2 UI)	Spec. In	Spec. In	1 UI = 404 ps
VdIVW_total	-	130 mV	Spec. In	Spec. In	Vcent_DQ = $\Delta VIHL/2$

Signal Integrity Test Result (Data strobe / Data)

■ tDQSS_U3_DQSL



■ tDQSS_U3_DQSU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQSL	DQSU	
tDQSS	-226 (-0.27tCK)	226 (+0.27tCK)	-44ps	-53ps	Spec. in

Thank you